



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:
Chen et al.

Serial No. 10/712,460

Filed: 11/13/2003

For: Semiconductor Wafer
Manufacturing Methods
Employing Cleaning Delay Period

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Group Art Unit: 1746

Examiner: To be determined

Customer No.: 000042717

Attorney Docket No.:
TSMC2002-1015/24061.42

SECOND INFORMATION DISCLOSURE STATEMENT

Mail Stop Amendment
Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In compliance with the duty of disclosure under 37 CFR §1.56, and in accordance with the practice under 37 CFR §1.97 and §1.98, the Examiner's attention is directed to the documents listed on the enclosed modified Form PTO-1449. No inference should be made that the cited references are in fact material, are in fact prior art, or that no better art exists. The cited patents are listed in numerical order and are not in any order based on their pertinence.

The above-identified application was filed after June 30, 2003. Therefore, pursuant to the waiver of the requirement under 37 CFR 1.98 (a)(2)(i) as stated in a Pre-OG Notice dated July 11, 2003, only a copy of the non-patent literature document listed on the enclosed modified Form PTO-1449 is attached.

This Information Disclosure Statement is being filed within three months of the United States filing date or before the mailing date of a first Office Action on the merits. No certification or fee is required (37 CFR §1.97(b)).

It is respectfully requested that the above information be considered by the Examiner and that a copy of the enclosed Form PTO-1449 be returned indicating that such information has been considered.

Respectfully submitted,

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R87496.1

Certificate of Mailing

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Commissioner For Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on 10-7-04.

Bonnie E. Boyle

